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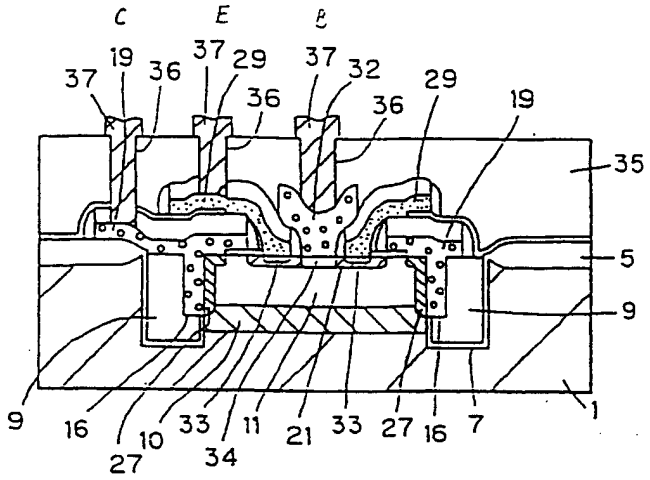
(54) Bipolar transistor with a reduced collector series resistance and method for fabricating the same

(57) A collector diffusion layer is provided in a bipolar transistor, wherein said collector diffusion layer (27) has a high impurity concentration and vertically extends along inside vertical walls of a vertical portion of a collector plug electrode (19), and said collector diffusion layer (27) extends from a surface region of a substrate into at least an intermediate level of a burying layer highly doped with the same impurity as that of said collector diffusion layer (27).

FIG. 3A



1 : p-type semiconductor substrate
5 : field oxide film
7 : trench groove
9 : trench isolation
10 : n^+ burying layer
11 : n-well layer
16 : contact hole
17 : polysilicon film
19 : collector plug electrode
21 : intrinsic base region
27 : collector diffusion layer
29 : emitter plug electrode
32 : base plug electrode
33 : emitter diffusion layer
34 : graft base layer
36 : contact holes
37 : electrode interconnection

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Description

The present invention relates to a bipolar transistor with a reduced collector series resistance and a method for fabricating the same.

In conventional fabrication methods for the bipolar transistors, a burying layer is formed on a semiconductor substrate and an epitaxial layer is grown on the burying layer. In order to shorten these conventional fabrication processes for the bipolar transistors, it was, however, proposed to form an n-type highly doped diffusion layer by an ion-implantation at a high energy in the range of 1MeV to 2MeV. In this method, a n-type burying layer and an n-type well layer overlying the n-type burying layer may be formed by use of the same mask but at different ion-implantation energies. This may shorten the fabrication processes for the bipolar transistors. This method for fabricating the bipolar transistor will be described with reference to FIGS. 1A and 1B.

FIG. 1A is a cross sectional elevation view illustrative of the conventional bipolar transistor wherein the n-type burying layer and the n-well layer overlaying the n-type burying layer have been formed by ion-implantation at different energies by use of the same mask.

FIG. 1B is a plane view illustrative of the conventional bipolar transistor illustrated in FIG. 1A.

The bipolar transistor is formed on a p-type semiconductor substrate 201. Trench isolations 209 are formed within trench grooves 207 formed in the p-type semiconductor substrate 201 so that the bipolar transistor is formed in a region surrounded by the trench isolations 209. An n^+ burying layer 210 is formed in the p-type semiconductor substrate surrounded by the trench isolations 209 by an ion-implantation of n-type impurity at a high ion-implantation energy. An n-well region 211 is then formed, which overlies the n^+ burying layer 210 by a subsequent ion-implantation of n-type impurity at an ion-implantation energy lower than the ion-implantation energy used for forming the n^+ burying layer 210. Field oxide films are selectively formed on a surface of the substrate. A p-type intrinsic base region 221 is formed in an upper region of the n-well region 211. A collector diffusion layer 227 is selectively formed in an upper portion of the n-well region 211. The collector comprises the n^+ burying layer 210, the n-well region 211, and the collector diffusion layer 227.

Graft base regions 234 are formed to surround the intrinsic base region 221. Base plug electrodes 232 are formed, which are in contact with the graft base regions 234. An emitter region 233 is formed in an upper portion of the intrinsic base region 221 to form a vertical n-p-n structure. The emitter diffusion region 233 may be formed by a diffusion of n-type impurity from an emitter plug electrode 229 into the intrinsic base region 221. Electrode interconnections 237 are formed in contact holes to be made into contact with the base plug electrodes 232, the emitter plug electrode 229 and the collector diffusion layer 227.

In the above bipolar transistor, a current flows downwardly from the collector diffusion layer 227 through the n-well region 211 to the n^+ burying layer 210 and then flows laterally through the n^+ burying layer 210 for subsequent flowing upwardly from the n-well region 211 to the intrinsic base region 221. When the bipolar transistor is placed in an active state, a space charge region extends under the intrinsic base region 221 and over the n^+ burying layer 210. Namely, the intrinsic base region 221 is connected through the space charge region to the n^+ burying layer 210. The space charge region is extremely lower in effective resistivity to current than the n-well region 211. Further, since the n^+ burying layer 210 is higher in impurity concentration than the n-well region 211, the n^+ burying layer 210 is much lower in effective resistivity to current than the n-well region 211. Current tends to flow through a region having a lower resistivity than other region surrounding the region, for which reason the current flows on a current pass which extends through the n-well region 211 as short as possible but through the n^+ burying layer 210 as long as possible. As a result, the current pass extends downwardly from the collector diffusion region 227 through the n-well region 211 to the n^+ burying layer 210 and further extends laterally through the n^+ burying layer 210 and moreover extends upwardly from the n^+ burying layer 210 through the space charge reign to the intrinsic base region 221. In the current pass described above, the space charge region and the n^+ burying layer 210 are much lower in effective resistivity to current than the n-well region, for which reason an effective collector series resistance is defined mostly by the resistance of the n-well region 211 under the collector diffusion region 227. Since the thickness of the n-well region 211 is determined in consideration of a base-collector withstand voltage, it is limited to reduce the thickness thereof. The collector series resistance of the above bipolar transistor is, therefore, substantially defined by the resistance of the n-well region 211 when the current flows from the collector diffusion region 227 to the n^+ burying layer 210 downwardly. As described above, the resistivity is defined by the impurity concentration. The n^+ burying layer 210 has a high impurity concentration in the order of 1×10^{19} atoms/cm^3, whilst the n-well region 211 has a lower impurity concentration in the order of 1×10^{13} atoms/cm^3. If, in order to reduce the resistivity of the n-well region 211, the impurity concentration of the n-well region 211 is risen up, then this raises problems with crystal defects caused by crystal damages in ion-implantation at high dose. Remarkable crystal defects cause leakage of current between collector and base or between emitter and collector.

In the above circumstances, it was practically difficult to reduce the collector series resistance to less than 100 Ω. If the collector series resistance is not sufficiently reduced and the bipolar transistor is made operate in a large collector current region, then the bipolar transistor is likely to be saturated or a cut off frequency is dropped,

thereby the required good properties can not be obtained.

In order to settle the above problems with a high collector series resistance, there was proposed another bipolar transistor with a lateral n-p-n structure in place of the above vertical n-p-n structure. Typical one of the conventional lateral n-p-n structure bipolar transistors will be described with reference to FIGS. 2A and 2B. This conventional lateral n-p-n structure bipolar transistor is disclosed in the Japanese laid-open patent publication No. 64-15973.

FIG. 2A is a cross sectional elevation view illustrative of the conventional bipolar transistor wherein a highly doped n-type collector diffusion layer is formed to laterally surround an n-type epitaxial layer which surrounds an intrinsic base region so that a collector plug electrode is connected via the n-type highly doped collector diffusion layer to a highly doped n-type burying layer whereby currents flow from the collector plug electrode through the n-type highly doped collector diffusion layer to the highly doped n-type burying layer.

FIG. 2B is a plane view illustrative of the conventional bipolar transistor illustrated in FIG. 2A.

On a p-type semiconductor substrate 301, field oxide films 304 are selectively formed to define an active region on which a bipolar transistor is formed. A highly doped n-type collector diffusion layer 306 is formed to laterally surround an n-type epitaxial layer 303 which surrounds an intrinsic base region 307. A ring-shaped emitter region 309 is formed in an upper portion of the intrinsic base region 307. A collector plug electrode 305 is formed in contact with the n-type highly doped collector diffusion layer 306. An n^+ burying layer 302 is formed under the intrinsic base region 307 and under the n-type highly doped collector diffusion layer 306 so that the collector plug electrode 305 is connected via the n-type highly doped collector diffusion layer 306 to the n^+ burying layer 302. Currents flow from the collector plug electrode 305 through the n-type highly doped collector diffusion layer 306 to the n^+ burying layer 302. The currents then laterally flow through the n^+ burying layer 302 and thereafter upwardly flow through a space charge region formed under the intrinsic base region 307 to the intrinsic base region 307, wherein the space charge region is formed only when the bipolar transistor is in active state. The current pass comprises the n-type highly doped collector diffusion layer 306, the n^+ burying layer 302 and the space charge region under the intrinsic base region 307. Namely, the current pass is free of a highly resistive region, for which reason the collector series resistance of the bipolar transistor illustrated in FIGS. 2A and 2B is lower as compared to that illustrated in FIGS. 1A and 1B. The bipolar transistor illustrated in FIGS. 2A and 2B is, however, engaged with a limitation to lateral scale down due to the following reasons.

The n-type highly doped collector diffusion layer 306 is formed by a diffusion of n-type impurity from the collector plug electrode 305 into the n-type epitaxial layer 303. The diffusion is continued until the impurity reaches the top of the n^+ burying layer 302 whereby the collector plug electrode 305 is connected via the n-type highly doped collector diffusion layer 306 to the n^+ burying layer 302. Since the impurity diffusion is isotropic, not only the vertical diffusion but also a lateral diffusion are caused. In consideration of the structure of the bipolar transistor, it is required that the n-type highly doped collector diffusion layer 306 is separated by the n-type epitaxial layer 303 from the intrinsic base region 307. Notwithstanding, the lateral diffusion of impurity from the collector plug electrode 305 forms the n-type highly doped collector diffusion layer 306 which laterally extends from the collector plug electrode 305 toward the intrinsic base region 307. Accordingly, it is essential that the collector plug electrode 305 is spaced in a lateral direction from the intrinsic base region 307 by a distance larger than a lateral diffusion distance. This provides a limitation to the lateral scaling down of the bipolar transistor. The above diffusion process may also provide a limitation to increase in impurity concentration of the collector diffusion layer 306. Namely, it is difficult to render the collector diffusion layer 306 to possess an impurity concentration so high as the n^+ burying layer 302. This limitation to the increase in the impurity concentration of the collector diffusion layer 306 results in a limitation to a reduction in collector series resistance of the bipolar transistor.

In the above circumstances, it had been required to develop an improved bipolar transistor having a substantially reduced collector series resistance and also having a structure suitable for a substantial space down in lateral directions.

Accordingly, it is an object of the present invention to provide an improved bipolar transistor free from any problems as described above.

It is a further object of the present invention to provide an improved bipolar transistor having a substantially reduced collector series resistance.

It is a further more object of the present invention to provide an improved bipolar transistor having a structure suitable for a substantial space down in lateral directions.

It is another object of the present invention to provide a novel method for forming an improved bipolar transistor free from any problems as described above.

It is still another object of the present invention to provide a novel method for forming an improved bipolar transistor having a substantially reduced collector series resistance.

It is yet another object of the present invention to provide a novel method for forming an improved bipolar transistor having a structure suitable for a substantial space down in lateral directions.

It is further another object of the present invention to provide a novel method for forming a trench groove in a semiconductor substrate, which is applicable to the fabrication of the bipolar transistor.

The above and other objects, features and advantages of the present invention will be apparent from the following descriptions.

The present invention provides a collector diffusion layer in a bipolar transistor, wherein said collector diffusion layer (27) has a high impurity concentration and vertically extends along inside vertical walls of a vertical portion of a collector plug electrode (19), and said collector diffusion layer (27) extends from a surface region of a substrate into at least an intermediate level of a burying layer highly doped with the same impurity as that of said collector diffusion layer (27).

The present invention also provides a method for forming a collector diffusion layer comprising the step of a thermal diffusion of impurity in a lateral direction from a vertical portion of a collector plug electrode (19) toward a well region surrounded by said collector plug electrode (19) so that said collector diffusion layer (27) has a high impurity concentration and vertically extends along inside vertical walls of a vertical portion of a collector plug electrode (19), and said collector diffusion layer (27) extends from a surface region of a substrate into at least an intermediate level of a burying layer highly doped with the same impurity as that of said collector diffusion layer (27).

Preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

FIG. 1A is a fragmentary cross sectional elevation view illustrative of the conventional bipolar transistor wherein the n-type burying layer and the n-well layer overlaying the n-type burying layer have been formed by ion-implantation at different energies by use of the same mask.

FIG. 1B is a fragmentary plane view illustrative of the conventional bipolar transistor illustrated in FIG. 1A.

FIG. 2A is a fragmentary cross sectional elevation view illustrative of the conventional bipolar transistor wherein a highly doped n-type collector diffusion layer is formed to laterally surround an n-type epitaxial layer which surrounds an intrinsic base region so that a collector plug electrode is connected via the n-type highly doped collector diffusion layer to a highly doped n-type burying layer whereby currents flow from the collector plug electrode through the n-type highly doped collector diffusion layer to the highly doped n-type burying layer.

FIG. 2B is a fragmentary plane view illustrative of the conventional bipolar transistor illustrated in FIG. 2A.

FIG. 3A is a fragmentary cross sectional elevation view illustrative of an improved bipolar transistor in a first embodiment according to the present invention.

FIG. 3B is a fragmentary plane view illustrative of the conventional bipolar transistor illustrated in FIG. 3A.

FIGS. 4A through 4O are fragmentary cross sectional elevation view illustrative of an improved bipolar transistors in sequential steps involved in a novel fabrication method therefor in a first embodiment according to the present invention.

FIG. 5 is a view showing a reduced collector series resistance of an improved bipolar transistor in accordance with the present invention as compared to collector series resistance of the two conventional bipolar transistors illustrated in FIGS. 1A, 1B, 2A and 2B.

FIG. 6 is a fragmentary cross sectional elevation view illustrative of an improved bipolar transistor in a second embodiment according to the present invention.

FIGS. 7A through 7N are fragmentary cross sectional elevation view illustrative of an improved bipolar transistors in sequential steps involved in a novel fabrication method therefor in a second embodiment according to the present invention.

A first embodiment according to the present invention will be described with reference to the accompanying drawings. FIG. 3A is a fragmentary cross sectional elevation view illustrative of an improved bipolar transistor in a first embodiment according to the present invention. FIG. 3B is a fragmentary plane view illustrative of the conventional bipolar transistor illustrated in FIG. 3A. FIGS. 4A through 4O are fragmentary cross sectional elevation view illustrative of an improved bipolar transistors in sequential steps involved in a novel fabrication method therefor in a first embodiment according to the present invention. The bipolar transistor is formed over a p-type semiconductor substrate 1. Field oxide films 5 are selectively formed on a surface of the p-type semiconductor substrate 1. Trench isolations 9 are formed in trench grooves 7 formed in the p-type semiconductor substrate 1 along edges of the field oxide films 5. The trench isolations 9 are made of silicon dioxide. The trench isolations 9 encompass an active region in which the bipolar transistor is formed. An n^+ burying layer 10 is formed in a deep portion of the p-type semiconductor substrate 1. The n^+ burying layer 10 laterally extends but is encompassed by the trench isolations 9. The bottom of the trench isolations 9 is deeper than the bottom of the n^+ burying layer 10. Collector plug electrodes 19 are formed, which comprises a horizontal portion laterally extending over the trench isolations 9 and outer portions of the active region encompassed by the trench isolations 9, and a vertical portion vertically extending along inside portions of the trench isolations 9. The vertical portions of the collector plug electrodes 19 are formed within contact holes 16 which have been formed along inside portions of the trench isolations 9 in the vertical direction from the top portion of the trench isolations 9 to a deeper portion but shallower than the bottom of the trench isolations 9. The bottom of the vertical portion of the collector plug electrodes 19 is positioned at almost an intermediate level of the n^+ burying layer 10. The inside edge of the vertical portion of the collector plug electrodes 19 is aligned to the inside edge of the trench isolations 9. Collector diffusion layers 27 are formed, which vertically extend along the inside walls of the vertical portions of the collector plug electrodes 19. The top of the collector diffusion layers 27 is positioned at the same level as the top of the vertical portion of the col-

lector plug electrodes 19. The bottom of the collector diffusion layers 27 is also positioned at the same level as the bottom of the vertical portion of the collector plug electrodes 19. The collector diffusion layers 27 laterally encompass an n-well region 11 which is positioned over the n^+ burying layer 10. An intrinsic base region 21 is selectively formed in an upper region of the n-well region 11. The intrinsic base region 21 is separated by the n-well region 11 from the collector diffusion layers 27 in the lateral direction and from the n^+ burying layer 10 in the vertical direction. A graft base layer 34 is formed at a center portion of the intrinsic base region 21. A base plug electrode 32 is formed in contact with the graft base layer 34. A ring-shaped emitter 33 is formed in an upper portion of the intrinsic base region 21. Emitter plug electrodes 29 are formed in contact with the ring-shaped emitter 33. The emitter plug electrodes 29 are separated by silicon oxide films from the collector plug electrodes 19. An inter-layer insulator 35 is formed over the bipolar transistor. Contact holes 36 are selectively formed in the inter-layer insulator 35. Electrode interconnections 37 are formed within the contact holes 36 formed in the inter-layer insulator 35 so that the electrode interconnections 37 are in contact with the collector plug electrodes 19, the base plug electrode 32 and the emitter plug electrodes 29 respectively.

As described above, the collector diffusion layers 27 are formed to vertically extend along the inside walls of the vertical portions of the collector plug electrodes 19. The collector diffusion layers 27 surrounds in the horizontal direction the n-well region 11. The collector diffusion layers 27 are formed by a thermal diffusion of impurity toward the n-well region 11 from the vertical portions of the collector plug electrodes 19, for which reason a thickness of the collector diffusion layers 27, namely a lateral size thereof may be controlled in the range of approximately 0.3 micrometers to approximately 0.5 micrometers. The collector diffusion layers 27 extends vertically from at the same level as the top of the n-well region 11 to the same level as the intermediate portion of the n^+ burying layer 10 so that the collector plug electrodes 19 is connected via the collector diffusion layers 27 to the n^+ burying layer 10. The collector plug electrodes 19 has an impurity concentration in the range of 1×10^{19} atoms/cm^3 to 1×10^{20} atoms/cm^3. The n-well region 11 has an impurity concentration in the range of 1×10^{16} atoms/cm^3 to 1×10^{17} atoms/cm^3. The impurity concentration of the collector diffusion layers 27 varies in the lateral direction. The impurity concentration of the collector diffusion layers 27 is dropped in a lateral direction toward the n-well region 11 from the same level as the collector plug electrodes 19 into the n-well region 11. The depth of the n^+ burying layer 10 is so determined that when the bipolar transistor is in an active state, then a space charge region formed under the intrinsic base region 21 extends to reach the n^+ burying layer 10. When the bipolar transistor enters into the on state, then a current flows from the collector plug electrodes 19 through the collector diffusion layers 27 into the n^+ burying layer 10. Since the impurity concentration of the collector diffusion layers 27 is higher at an interface to the inside wall of the vertical portion of the collector plug electrodes 19, the majority of the current flows through the collector diffusion layers 27 but a high impurity concentration region thereof near the interface thereof to the collector plug electrodes 19. Subsequently, the current laterally flows through the n^+ burying layer 10 and then flows upwardly through the space charge region formed over the n^+ burying layer 10 and under the intrinsic base region 21 to the intrinsic base region 21. The collector plug electrodes 19, the collector diffusion layers 27, and the n^+ burying layer 10 have high impurity concentrations. The current pass comprises the collector plug electrodes 19, the collector diffusion layers 27, and the n^+ burying layer 10 and further the space charge region, for which reason the collector series resistance is substantially reduced. FIG. 5 is a view showing a reduced collector series resistance of the above improved bipolar transistor in accordance with the present invention as compared to collector series resistances of the two conventional bipolar transistors illustrated in FIGS. 1A, 1B, 2A and 2B. The collector series resistance of the improved bipolar transistor in accordance with the present invention is one tenth of that of the first conventional bipolar transistor illustrated in FIGS. 1A and 1B and is one fourth of that of the second conventional bipolar transistor illustrated in FIGS. 2A and 2B.

The existence of the collector diffusion layers 27 ensures a sufficiently large section area for the current passes between the collector plug electrodes 19 and the n^+ burying layer 10. This suppresses any increase in the collector series resistance of the bipolar transistor.

Further, as described above, in accordance with the present invention, the thickness of the collector diffusion layer 27, namely the horizontal size of the collector diffusion layer 27 may be limited in the range of about 0.3 micrometers to 0.5 micrometers. This allows that the collector plug electrodes 19 is formed relatively near the intrinsic base region 21 so that the collector diffusion layer 27 may approach toward the intrinsic base region 21 in the lateral direction by a distance in the range of 0.8 micrometers to 0.4 micrometers as compared to that of the conventional bipolar transistor. This may reduce the lateral size of the bipolar transistor by 20% to 30% as compared to the conventional bipolar transistor. By contrast, in the second conventional bipolar transistor illustrated in FIGS. 1A and 1B, the horizontal size of the collector diffusion layer 306 is 1.2 micrometers to 0.9 micrometers when the depth of the n^+ burying layer 302 from the surface of the substrate is 1.5 micrometers.

The above improved bipolar transistor may be fabricated as follows, wherein the above described invention may be applied to a BiCMOS device.

With reference to FIG. 4A, an oxide film 5 having a thickness of 10-50 nanometers is formed on a surface

of the p-type semiconductor substrate 1. A photo-resist mask is selectively formed over the oxide film 5 to be used for ion implantation of boron at a dose in the range of 1×10^{12} atoms/cm^3 to 1×10^{13} atoms/cm^3 at an acceleration energy in the range of 150 keV to 300 keV. The used photo-resist mask is then removed and in place another photo-resist mask is selectively provided over the oxide film 5 to be used for another ion implantation of phosphorus at a dose in the range of 1×10^{12} atoms/cm^3 to 1×10^{13} atoms/cm^3 at an acceleration energy in the range of 300 keV to 900 keV. The substrate 1 is subjected to a heat treatment in the nitrogen atmosphere at a temperature in the range of 1000°C to 1100°C for sixty minutes to thereby selectively form an n-type well region 3 and a p-type well region adjacent to the n-type well region 3 in the p-type semiconductor substrate 1. Thereafter, the used photo-resist mask is removed. A nitride film not illustrated and having a thickness in the range of 100-150 nanometers is formed over the oxide film 2. The nitride film is then selectively removed by a photo-etching technique. The remaining nitride film is used as a mask for a selective thermal oxidation to selectively form field oxide films 5 having a thickness in the range of 400-600 nanometers. The remaining nitride film is then removed.

With reference to FIG. 4B, a nitirde film 6 having a thickness in the range of 50-100 nanometers is formed on an entire surface of the substrate. The nitirde film 6 and the oxide film 2 are then selectively removed by a photo-etching technique. Subsequently, the p-type semiconductor 1 is then removed by a reactive ion etching which uses Cl_2/Ar/He mixing gases to form trench grooves 7. The nitride film is used as a mask for subsequent thermal oxidation to form oxide films 8 having a thickness in the range of 20-50 nanometers on vertical walls and bottoms of the trench grooves 7 formed in the -type semiconductor substrate 1.

With reference to FIG. 4C, an oxide film 9 is deposited by a chemical vapor deposition method so that the oxide film 9 extends entirely over the nitride film 6 and also within the trench grooves 7.

With reference to FIG. 4D, an anisotropic etching such as reactive ion etching to the oxide film 9 is then carried out to leave the oxide film 9 only within the trench grooves 7. In this etching process, it is preferable that a selective ratio to the nitride film is 40-50, namely an etching rate of the oxide film 9 is forty times to fifty times of the etching rate of the nitride film 6. It is, for example, available that CO/CHF_3 mixing gases are used to carry out the reactive ion etching so as to easily leave the oxide film 9 only within the trench grooves 7.

With reference to FIG. 4E, a hot phosphorus acid is used to remove the nitride film 6. A photolithography is used to form a photo-resist film having an opening which is positioned over a region surrounded by the trench grooves within which the remaining oxide films 9 are present. The photo-resist film is used as a mask for ion implantation of phosphorus at an acceleration energy of 1 MeV and a dose of 1×10^{14} atoms/cm^2 to form an n$^+$ burying layer 10 at a deep portion in the p-type semiconductor substrate 1. The above photo-resist film is again used as a mask for further ion implantation of phosphorus at an acceleration energy of 400 keV and a dose of 1×10^{13} atoms/cm^2 to form an n-well region 11 over the n$^+$ burying layer 10.

With reference to FIG. 4F, on a p-MOS region 12, phosphorus is ion-implanted into the n-well region 3 to adjust a threshold voltage. On an n-MOS region 13, boron is ion-implanted into the p-well region 4 adjust a threshold voltage. The oxide films 2 are removed to have the n-well region 3 and the p-well region 4 exposed as well as have the n-well region 11 exposed in a bipolar transistor region 14. A steam oxidation is carried out at a temperature of 800-900°C to form gate oxide films 15 having a thickness in the range of 5-10 nanometers over the n-well region 3 and the p-well region 4 as well as over the n-well region 11.

With reference to FIG. 4G, a photo-etching technique is used to selectively remove the oxide film 15 over the oxide films 9 within the trench grooves 7 and end portions of the n-well region 11 to expose the oxide films 9 and the end portions of the n-well region 11. The oxide films 9 and the oxide film 8 are selectively etched by an anisotropic etching such as a reactive ion etching to form contact holes 16 within the oxide films 9 but in the vicinity of the n-well region 11. The contact holes 16 vertically extend to the intermediate level in depth of the n$^+$burying layer 10. It is advantageously possible that a photo-mask alignment for forming the contact holes 16 may be made to align the opening of the photo-mask to extend side edges of the n-well region 11, for example, by 0.1-0.2 micrometers so that even if the photo-mask alignment has a slight displacement, then the side edges of the n$^+$burying layer 10 is securely exposed through the contact holes 16.

With reference to FIG. 4H, a polysilicon film 17 is entirely formed over the substrate so that the polysilicon film 17 extends over the gate oxide films 15, the field oxide films 5 and the top portions of the oxide films 9 within the trench grooves 7 and further within the contact holes 16 whereby the polysilicon film 17 is made into contact with the upper half portion of the side edges of the n$^+$burying layer 10. This polysilicon film 17 may be formed by a chemical vapor deposition method until the polysilicon film 17 has a thickness of 200 nanometers and subsequent ion implantation of n-type impurity such as phosphorus at an acceleration energy of 30 keV and at a dose of 1×10^{16} atoms/cm^2. This polysilicon film 17 may be replaced by a polyside film. Alternatively, it may be possible that the impurity may be introduced into the polysilicon film during the deposition of the polysilicon film 17. An inter-layer insulator 18 having a thickness of approximately 200 nanometers is then formed by a chemical vapor deposition. The inter-layer insulator 18 may be made of either silicon oxide or silicon nitride.

With reference to FIG. 4I, the polysilicon film 17 and

the inter-layer insulator 18 are selectively removed by a photo-etching technique to form collector plug electrodes 19 and gate electrodes 20. An intrinsic base region 21 is formed by an ion implantation of boron at an acceleration energy of 20 keV and at a dose of $5 \times 10^{13}cm^{-2}$ in a self-alignment method using the remaining inter-layer insulator 18 and the collector plug electrodes 19 as masks.

With reference to FIG. 4J, an insulation film made of either silicon oxide or silicon nitride is entirely formed over the substrate and then an anisotropic etching such as reactive ion etching is carried out to form side walls 22 at the sides of the gate electrode 20 and the sides of the collector plug electrodes. Oxide films 23 having a thickness of 10-20 nanometers are formed. A photo-resist film is used for subsequent ion implantation of arsenic at an acceleration energy of 50 keV an at a dose of $5 \times 10^{15}cm^{-2}$ to form source/drain regions 24 in the p-well region 4. The photo-resist film is removed and in place another photo-resist film is then formed for further ion implantation of BF_2 at an acceleration energy of 50 keV an at a dose of $5 \times 10^{15}cm^{-2}$ to form source/drain regions 25 in the n-well region 3. Alternatively, it is possible that prior to the formation of the side walls 22, preliminary ion implantation of arsenic and BF_2 at the acceleration energy of 50 keV but at a dose of $1 \times 10^{13}cm^{-2}$ to form lightly doped diffusion structures. It is further possible that the formation of the intrinsic base region 21 is formed after the side walls 22 are formed whereby the emitter diffusion regions may be formed within the intrinsic base region 21 due to a difference in diffusion coefficient between boron and arsenic.

With reference to FIG. 4K, n oxide film 26 having a thickness of 150 nanometers is entirely formed by a chemical vapor deposition method. An annealing is carried out in a nitrogen atmosphere at a temperature in the range of 850-900°C for 30 minutes to activate the impurities in the source/drain regions 24 and 25 as well as in the intrinsic base region 21 and further obtain a recovery of damages caused by the ion-implantation as well as cause an impurity diffusion from the vertical portion of the collector plug electrode 19 to the side portions of the n-well region 11 to thereby form the collector diffusion region 27. The junction depth of the intrinsic base region becomes 100-150 nanometers.

In the manner as well illustrated in FIGS. 4L through 4O, the bipolar transistor may be formed.

A second embodiment will be described in which the bipolar transistor structurally differ from that in the first embodiment in a depth of the bottom of the collector plug region and the bottom of the collector diffusion regions. The collector plug region and the collector diffusion regions are positioned below the bottom of the n+burying layer. This structure enlarges the area of the interface between the n+burying layer and the collector diffusion regions. This may reduce the collector series resistance. FIG. 6 is a fragmentary cross sectional elevation view illustrative of the improved bipolar transistor in this second embodiment according to the present invention. FIGS. 7A through 7N are fragmentary cross sectional elevation view illustrative of the improved bipolar transistors in sequential steps involved in a novel fabrication method therefor in this second embodiment according to the present invention. The above improved bipolar transistor may provide the same effects as what have been described in the first embodiment.

Claims

1. A collector diffusion layer in a bipolar transistor, wherein said collector diffusion layer (27) has a high impurity concentration and vertically extends along inside vertical walls of a vertical portion of a collector plug electrode (19), and said collector diffusion layer (27) extends from a surface region of a substrate into at least an intermediate level of a burying layer highly doped with the same impurity as that of said collector diffusion layer (27).

2. A method for forming a collector diffusion layer comprising the step of a thermal diffusion of impurity in a lateral direction from a vertical portion of a collector plug electrode (19) toward a well region surrounded by said collector plug electrode (19) so that said collector diffusion layer (27) has a high impurity concentration and vertically extends along inside vertical walls of a vertical portion of a collector plug electrode (19), and said collector diffusion layer (27) extends from a surface region of a substrate into at least an intermediate level of a burying layer highly doped with the same impurity as that of said collector diffusion layer (27).

FIG. 1A prior art

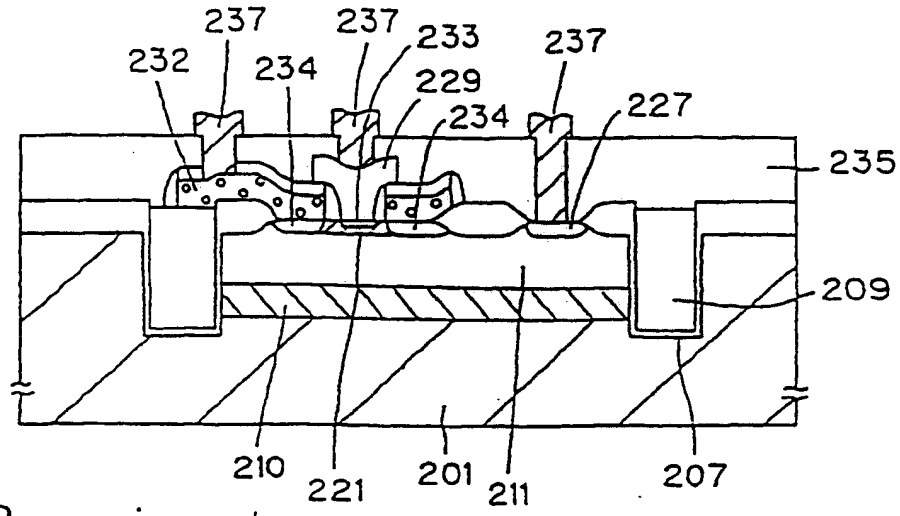
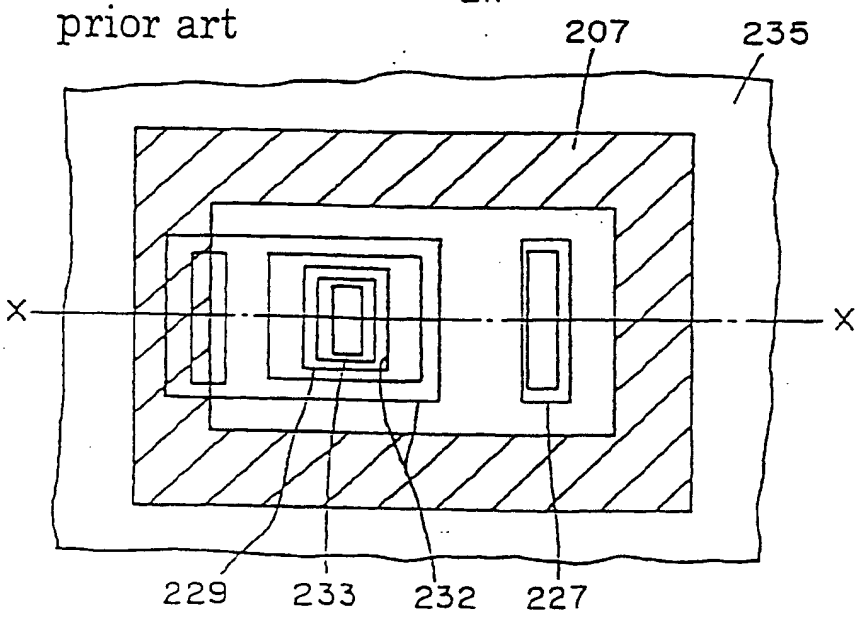


FIG. 1B prior art



201 : p-type semiconductor substrate
207 : trench groove
209 : trench isolation
210 : n^+ burying layer
211 : n-well layer
221 : intrinsic base layer
227 : collector diffusion layer
229 : emitter plug electrode
232 : base plug electrode
233 : emitter diffusion layer
234 : graft base layer
235 : inter-layer insulator
237 : electrode interconnection

FIG. 2A prior art

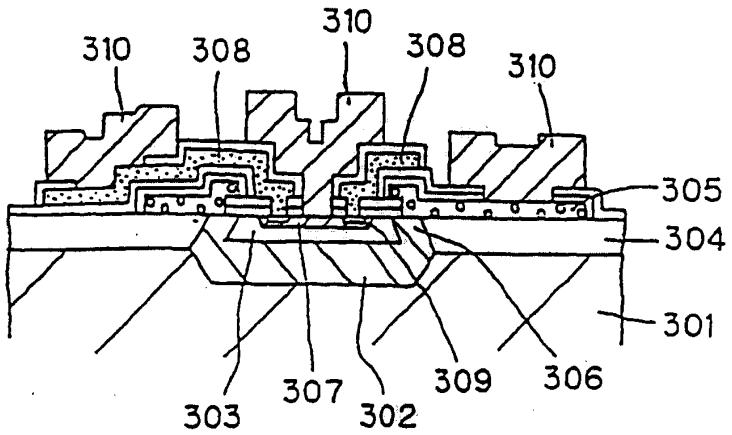
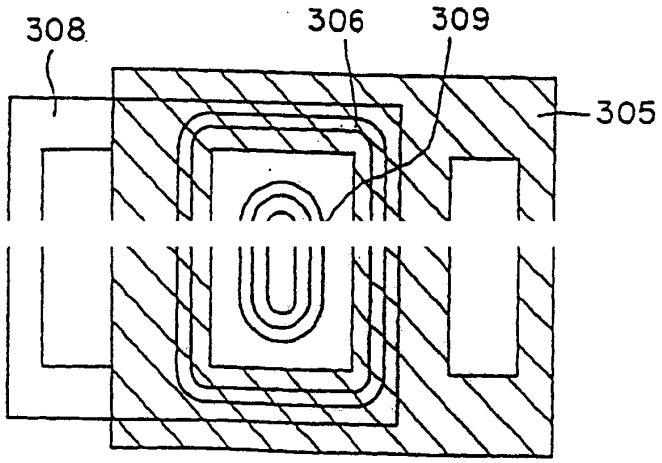


FIG. 2B prior art



301 : p-type semiconductor substrate
302 : n^+ burying layer
303 : n-type epitaxial layer
304 : isolation film
305 : collector plug electrode
306 : collector diffusion layer
307 : base region
308 : emitter plug electrode
309 : emitter diffusion layer
310 : electrodes

FIG. 3A

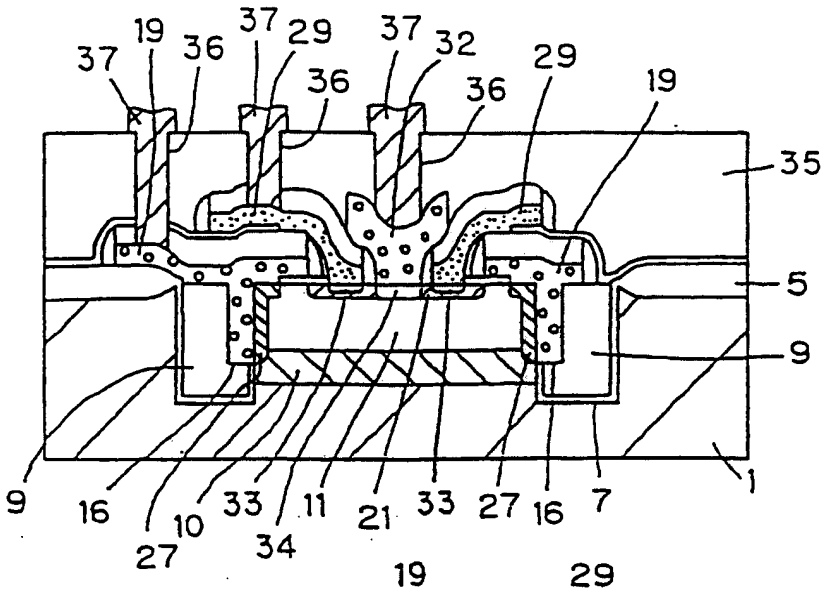
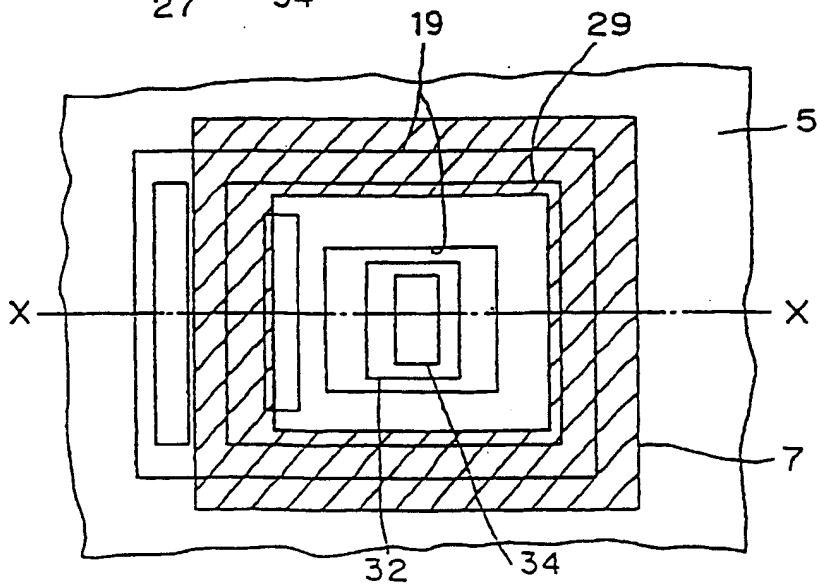


FIG. 3B



1 : p-type semiconductor substrate
5 : field oxide film
7 : trench groove
9 : trench isolation
10 : n^+ burying layer
11 : n-well layer
16 : contact hole
17 : polysilicon film
19 : collector plug electrode
21 : intrinsic base region
27 : collector diffusion layer
29 : emitter plug electrode
32 : base plug electrode
33 : emitter diffusion layer
34 : graft base layer
36 : contact holes
37 : electrode interconnection

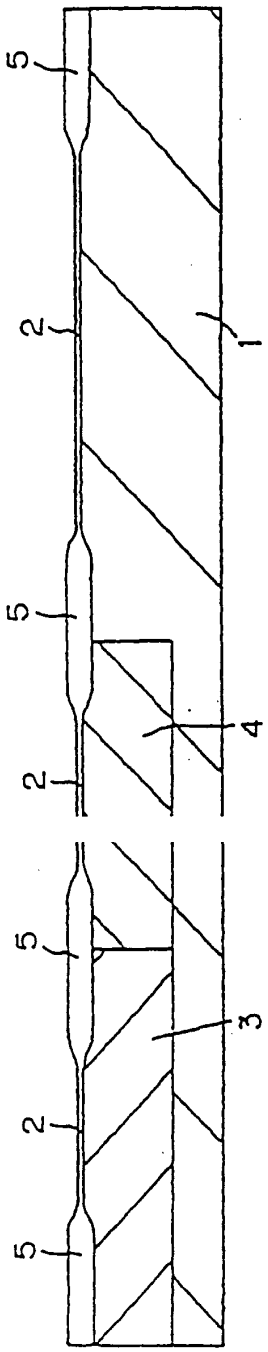


FIG. 4A

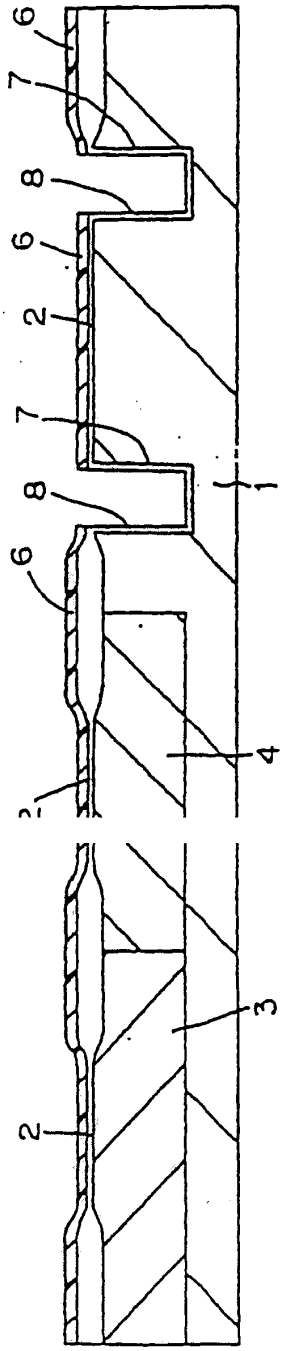


FIG. 4B

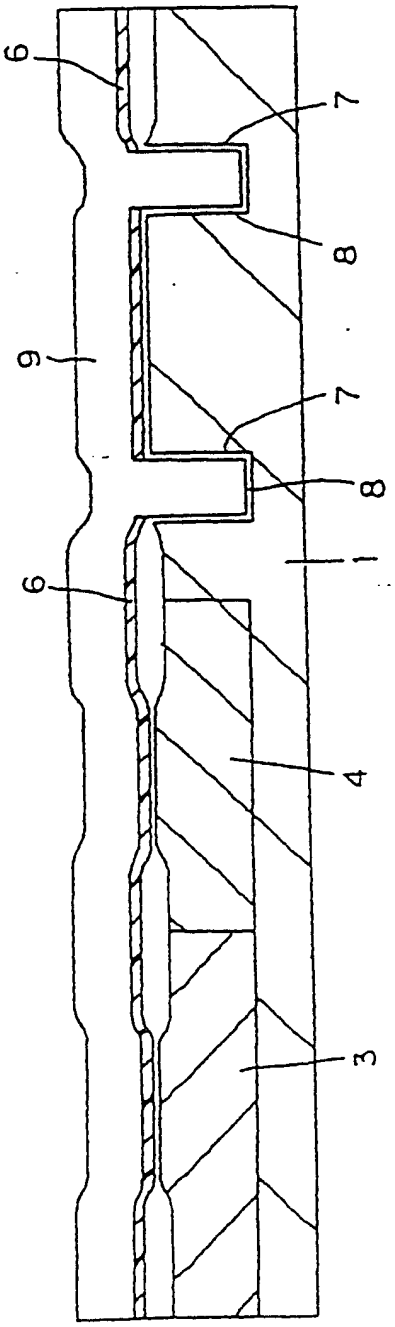


FIG. 4C

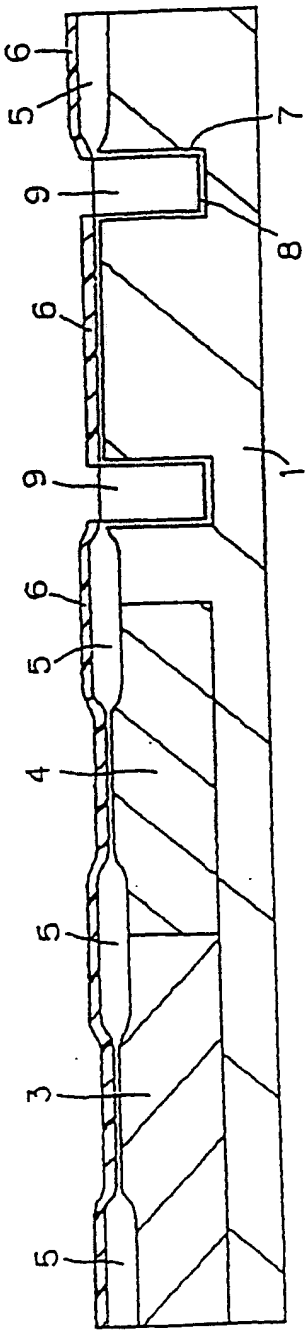
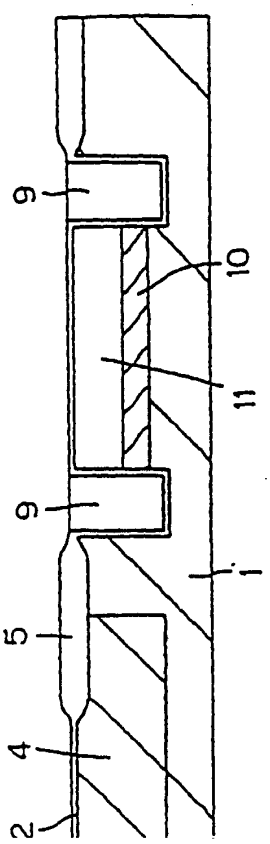


FIG. 4D



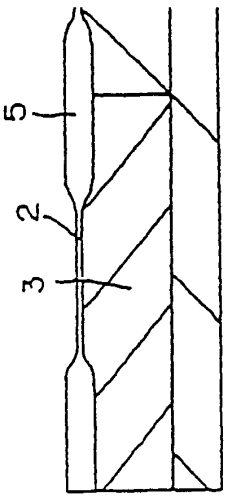
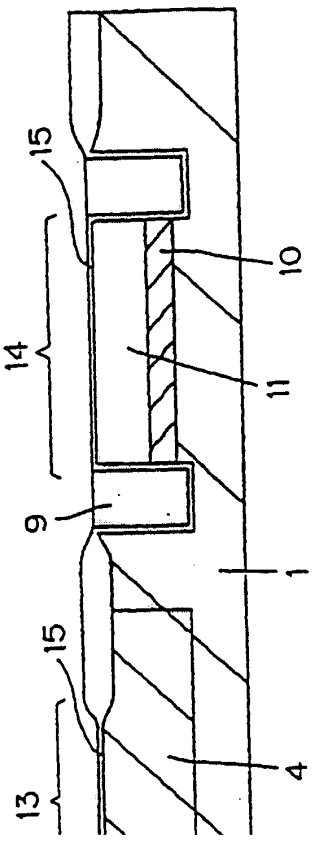


FIG. 4E



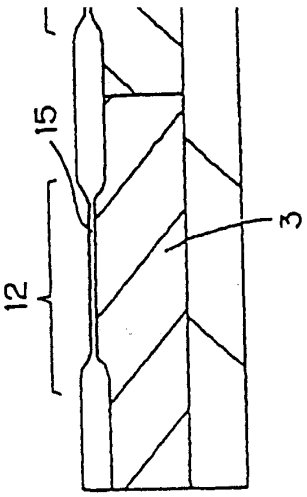


FIG. 4F

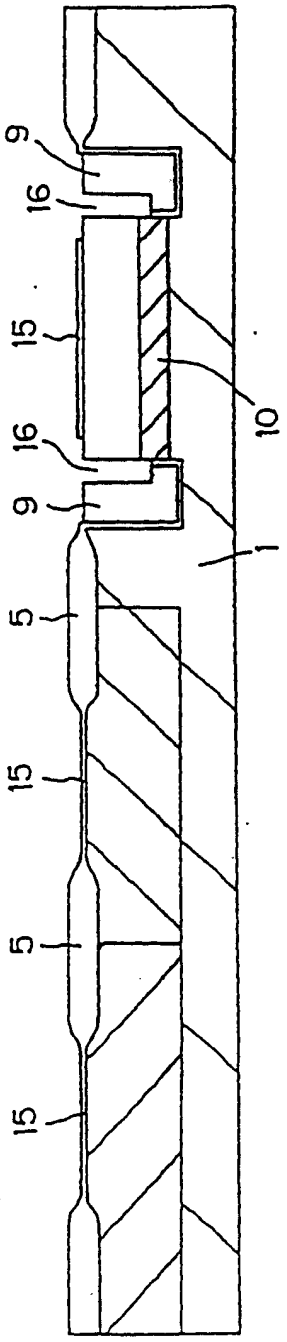


FIG. 4G

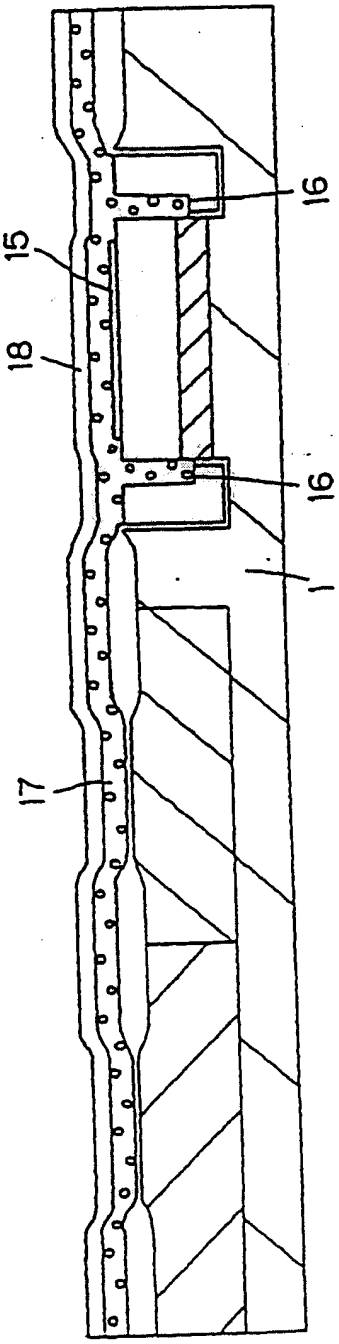
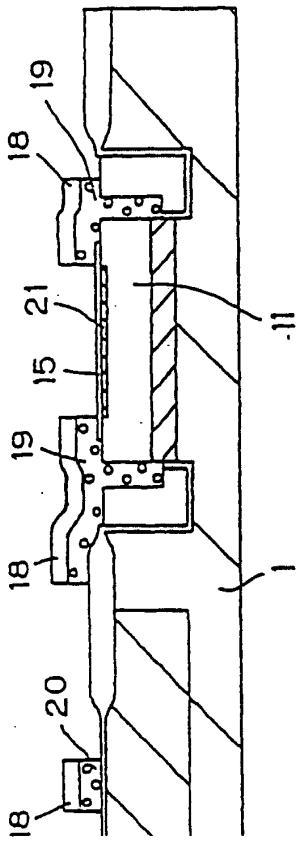


FIG. 4H


18
19
21
15
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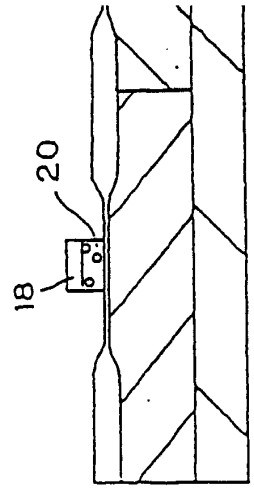
18
11
1

FIG. 4I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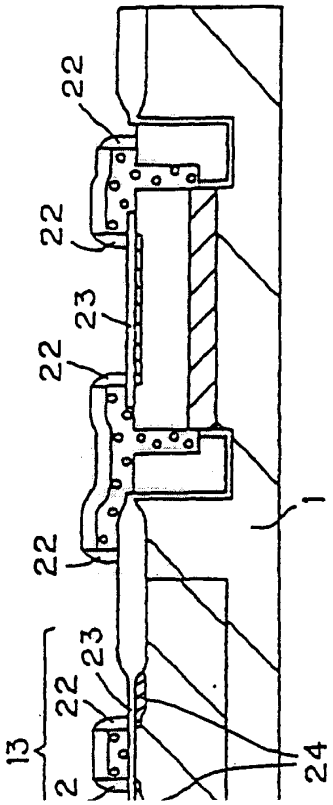
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23
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1
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2
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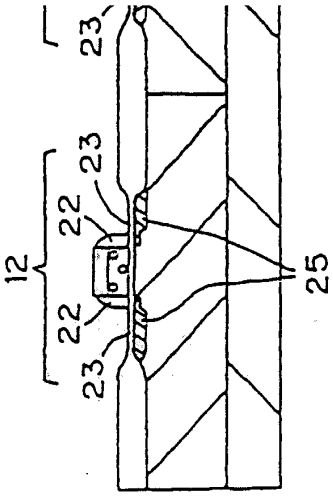
24

FIG. 4J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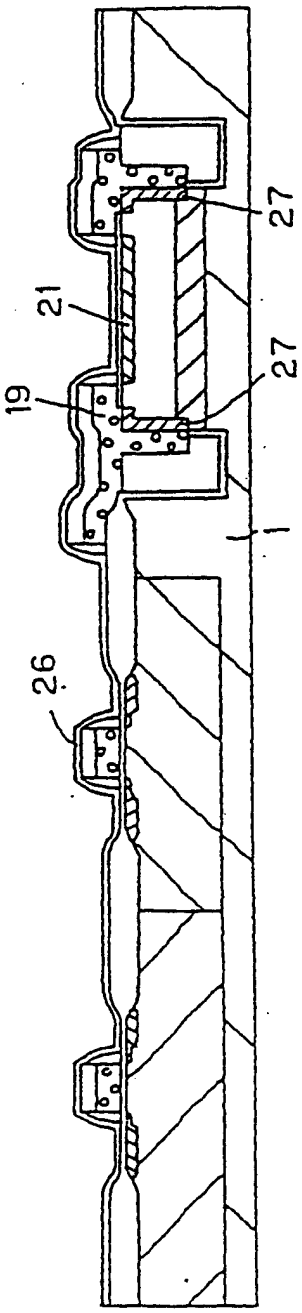


FIG. 4K

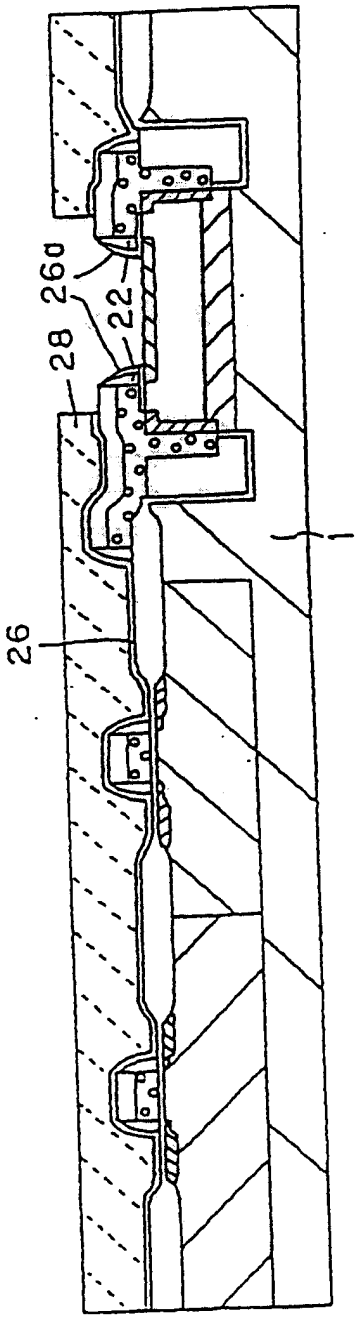


FIG. 4L

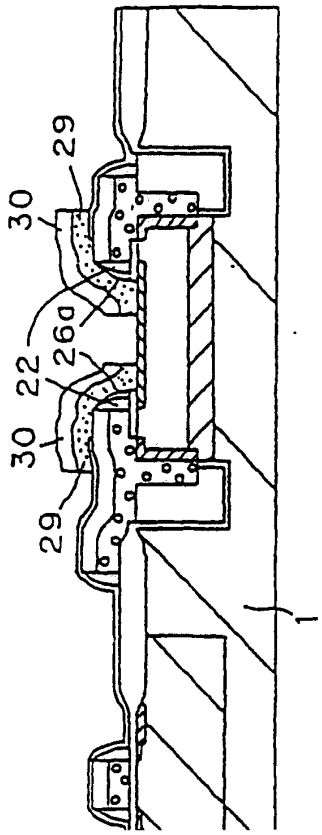


FIG. 4M

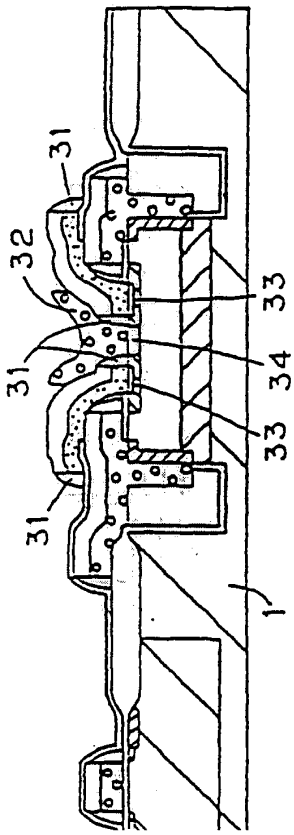


FIG. 4N

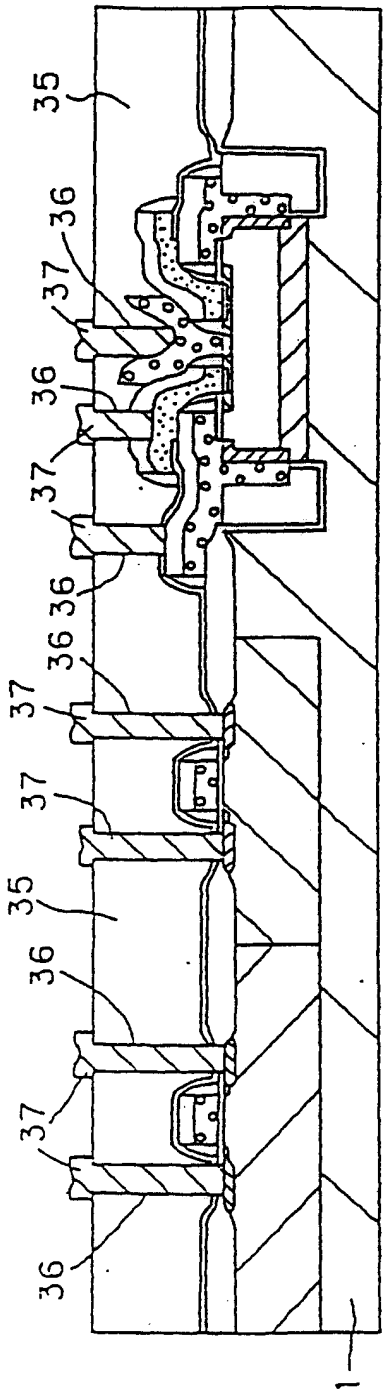


FIG. 40

FIG. 5

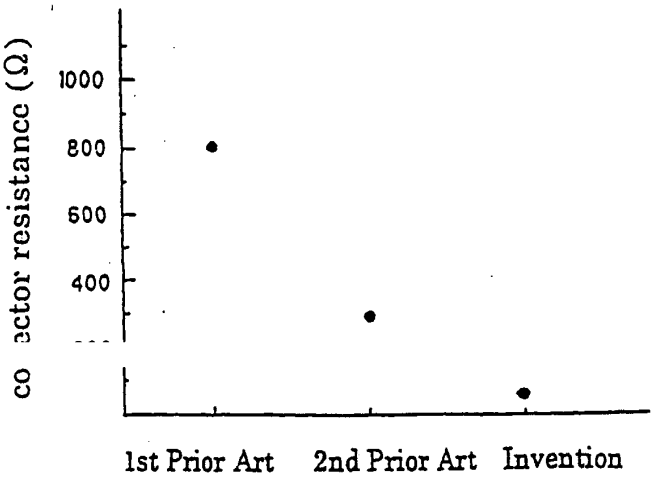
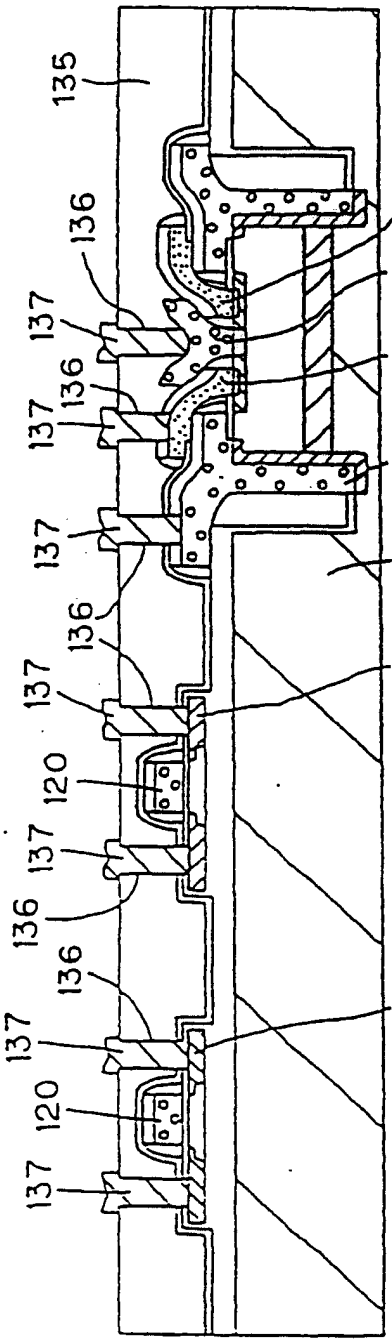

ɔctor resistance (Ω)
1000
800
600
400
1st Prior Art
2nd Prior Art
Invention

FIG. 6



101 : p-type semiconductor substrate
119 : collector plug electrode
120 : gate electrode
124, 125 : source/drain regions
129 : emitter plug electrode
132 : base plug electrode
133 : emitter diffusion layer

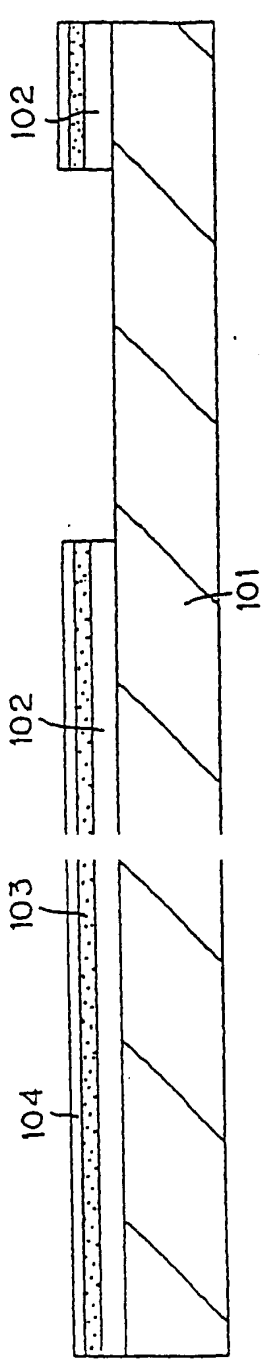


FIG. 7A

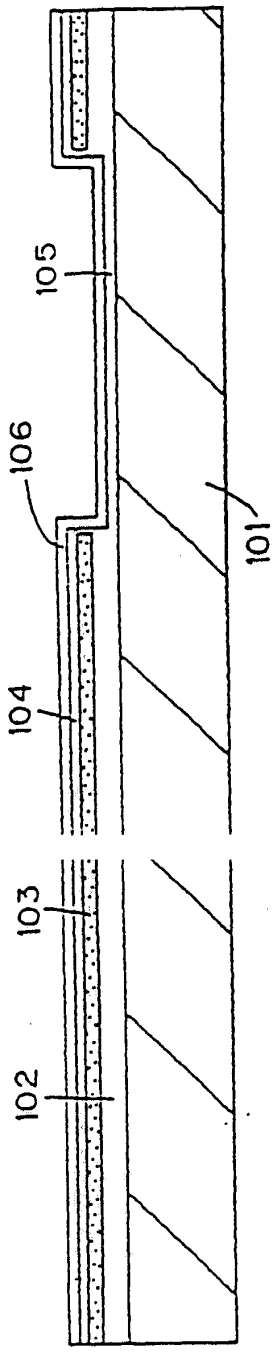


FIG. 7B

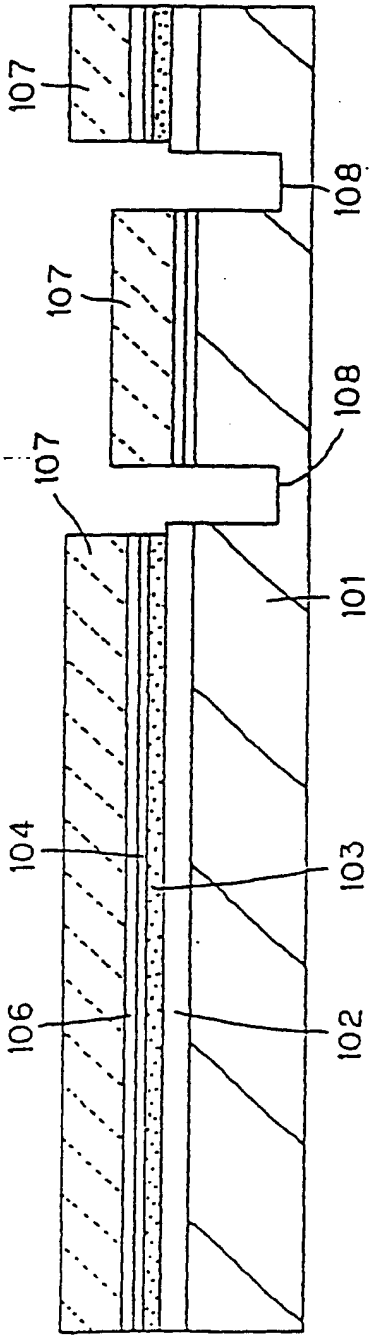

107
108
107
108
107
101
104
103
106
102

FIG. 7C

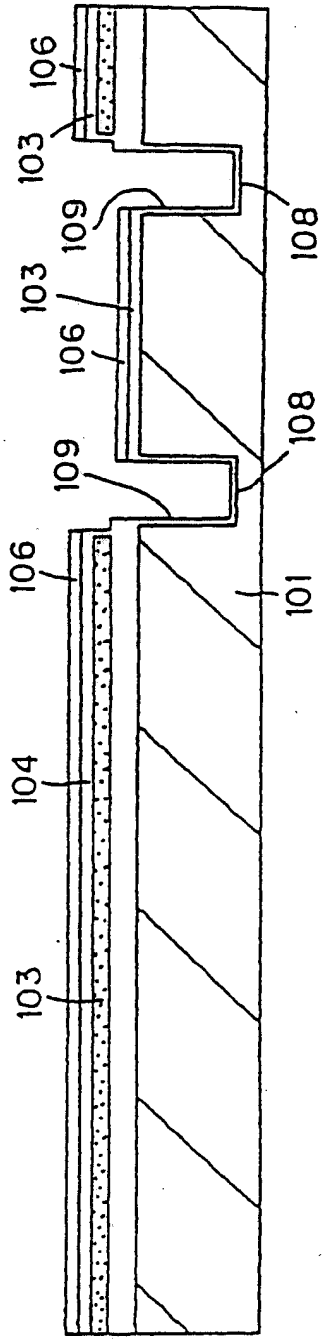

106
103
109
108
103
106
109
108
106
101
104
103

FIG. 7D

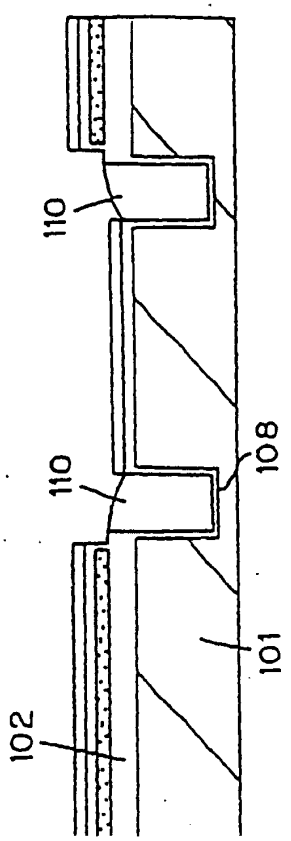

110
110
108
101
102
103
104
106

FIG. 7E

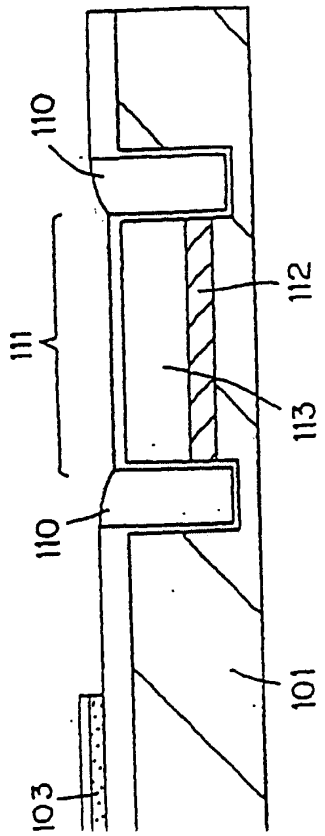

110
111
112
113
110
101
103
104
103

FIG. 7F

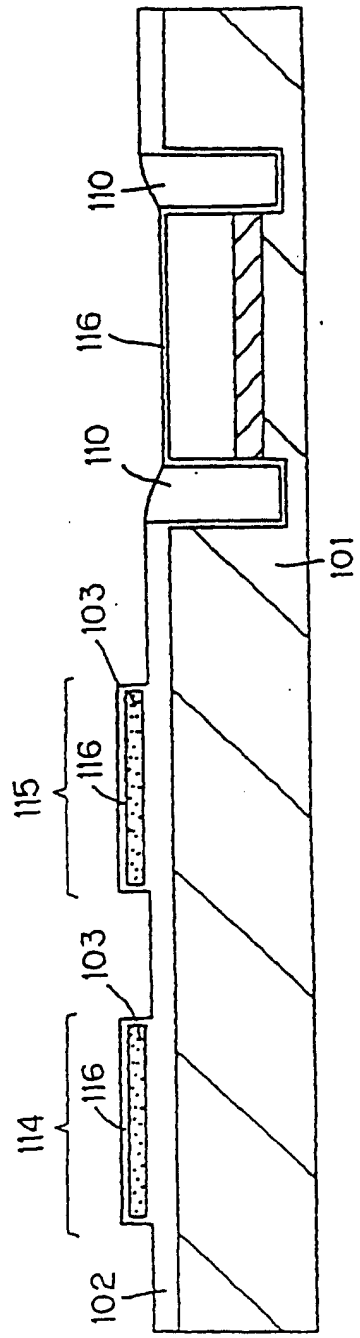

110
116
110
101
103
115
116
103
114
116
102

FIG. 7G

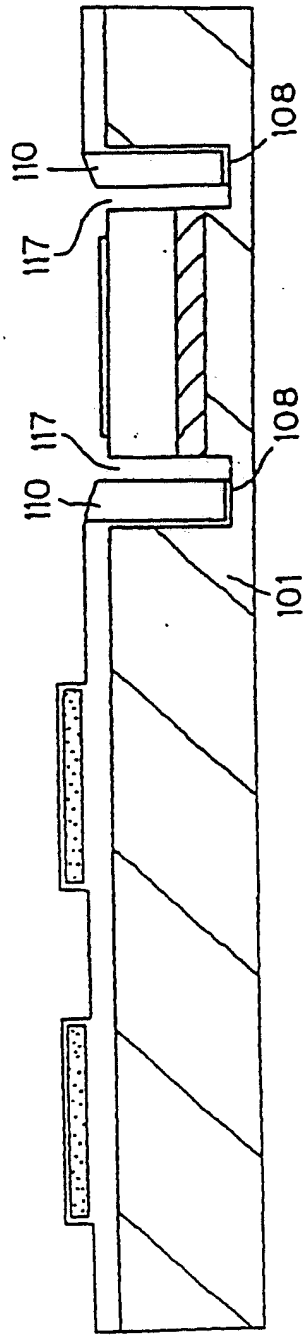
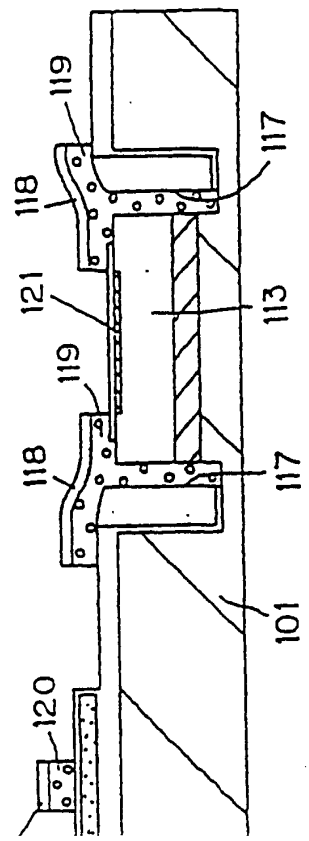

110
108
117
117
108
110
101

FIG. 7H


119
117
118
121
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119
118
117
101
120

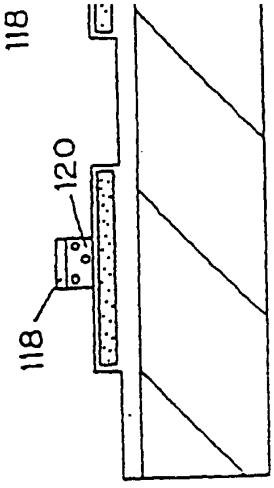
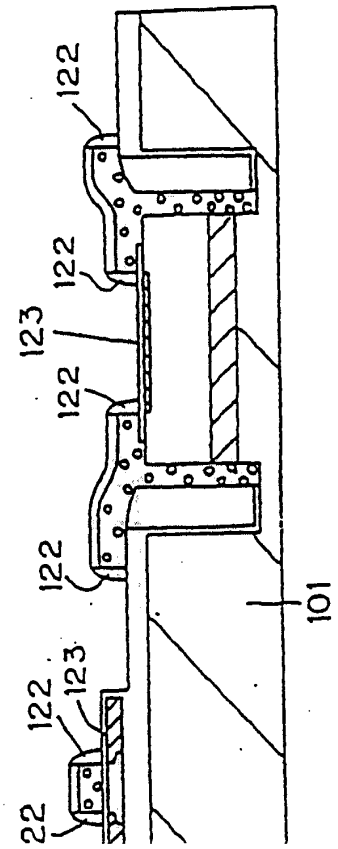

118
120
118

FIG. 7I


122
122
123
122
122
101
122
123
22

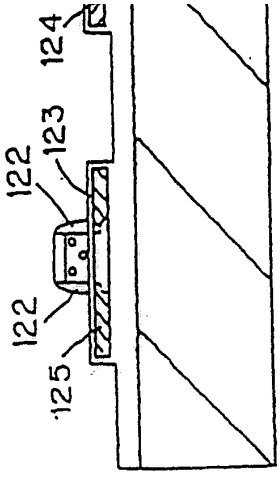

124
122
123
122
125

FIG. 7J

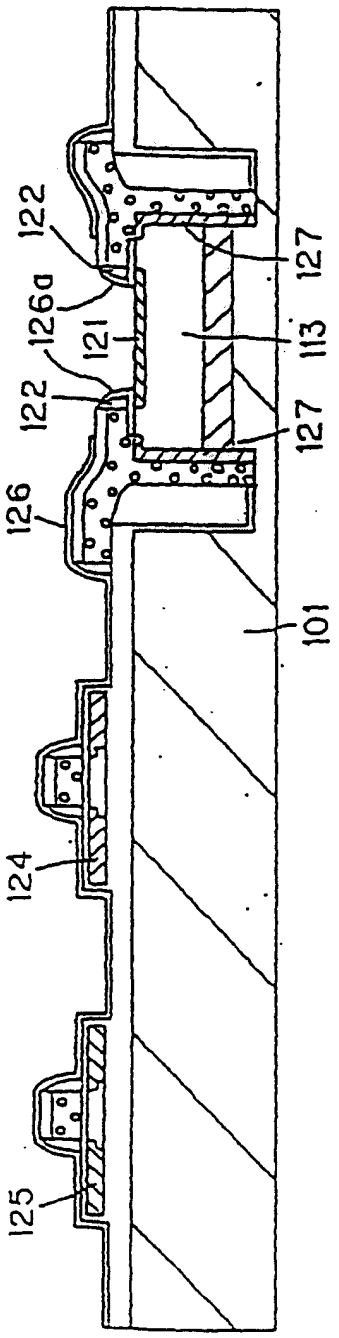

122
126a
121
122
126
124
125
127
113
127
101

FIG. 7K

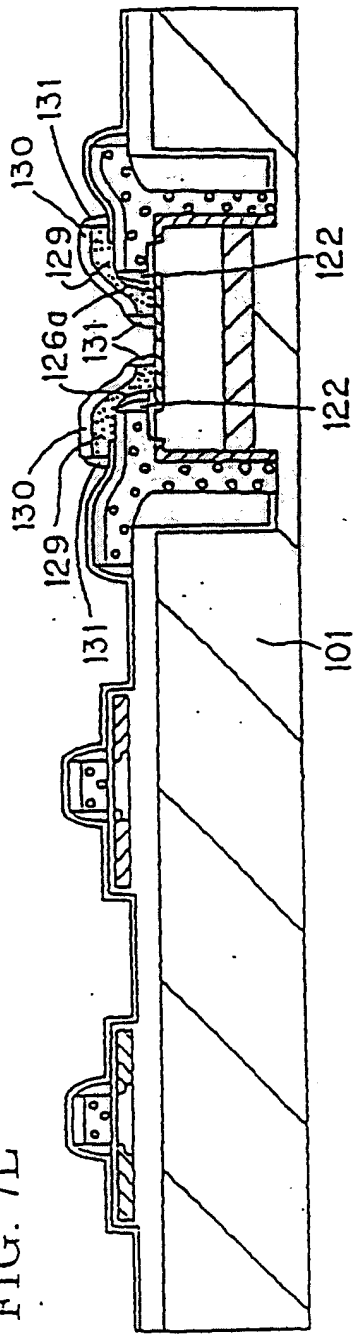

130
131
129
126a
131
130
129
131
122
122
101

FIG. 7L

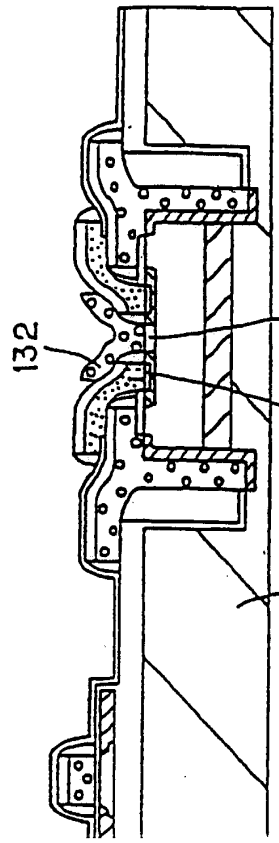
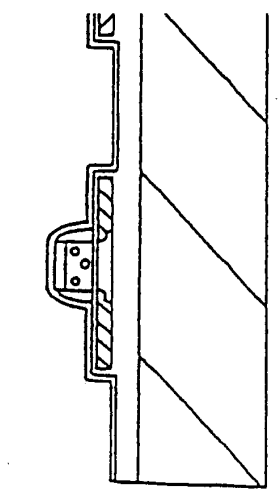
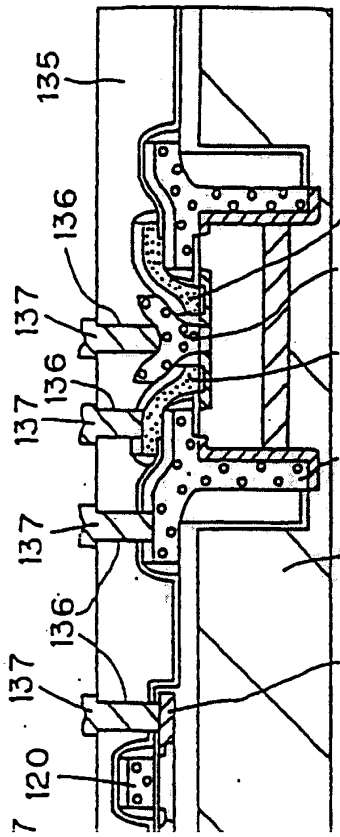


FIG. 7M





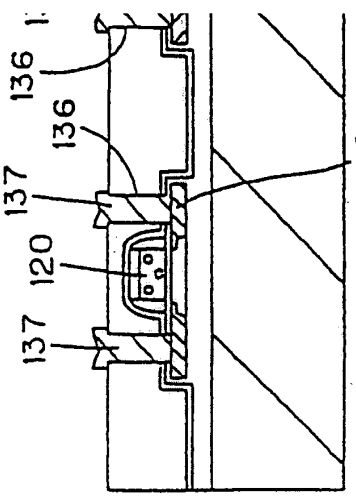


FIG. 7N

101 : p-type semiconductor substrate 12
119 : collector plug electrode 12
120 : gate electrode
125 : source/drain regions 132 : base plug electrode
: emitter plug electrode 133 : emitter diffusion layer

DOCKET NO: MUH 11086
SERIAL NO: 09/931,689
APPLICANT: Werner

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